REMARKS

This is a full and timely response to the outstanding non-final Office Action mailed March 28, 2008. The Examiner is thanked for the thorough examination of the present application. Upon entry of this response, claims 8-20 are pending in the present application. Applicants respectfully request consideration of the following remarks contained herein. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

I. Response to Claim Rejections Under 35 U.S.C. § 103

The USPTO has the burden under section 103 to establish a *prima facie* case of obviousness according to the factual inquiries expressed in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966). The four factual inquires, also expressed in MPEP §2141, are as follows:

(A) Determining the scope and contents of the prior art;

(B) Ascertaining the differences between the prior art and the claims in issue;

(C) Resolving the level of ordinary skill in the pertinent art; and

(D) Evaluating evidence of secondary considerations.

For a proper rejection of the claim under 35 U.S.C. §103, the cited combination of references must disclose, teach or suggest all elements / features of the claim at issue. See, e.g., *In re Dow Chemical*, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988) and *In re Keller*, 208 U.S.P.Q.2d 871, 881 (C.C.P.A. 1981). Claims 8-20 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over *Sah et al.* (U.S. Pat. No.

7,047,374, hereinafter "*Sah*") in view of *Ross* (U.S. Pub. No. 2004/0199729). For at least the reasons set forth below, Applicants traverse the rejections set forth.

Independent Claim 8

Applicants respectfully submit that independent claim 8 patently defines over *Sah* in view of *Ross* for at least the reason that the combination fails to disclose, teach or suggest the features emphasized below in claim 8.

Claim 8 recites:

> 8. A method of accessing Double Data Rate Synchronous Dynamic Random Access Memory (DDR SDRAM) memory storage employed in a packet switch, the DDR SDRAM memory having a plurality of memory banks for storing packet data of a plurality of packets, the method comprising steps of:
>
> a. ***segmenting packet data into variable size burst units***;
>
> b. ***sequencing a plurality of burst unit memory write operations ensuring that each burst unit memory write operation writes packet data to a memory bank different from the previous burst unit memory write operation***;
>
> c. sequencing a plurality of burst unit memory read operations ensuring that each bust unit memory read operation reads packet data from a memory bank different from the previous burst unit memory read operation;
>
> d. arranging the plurality of sequenced burst unit memory write operations in a plurality of write windows;
>
> e. arranging the plurality of sequenced bust unit memory read operations in a plurality of read windows; and
>
> f. performing memory access operations interleaving the write windows with the read windows.

(Emphasis added). On page 2, the Office Action alleges that the *Sah* reference discloses the steps emphasized above in claim 8. Applicants respectfully disagree. First, in alleging that *Sah* discloses ***segmenting packet data into variable size burst units***, the Office Action cites col. 7, line 15 in *Sah*. *Sah* discloses that "[t]he effective bandwidth achieved on the interface, in one embodiment, may depend upon the

distribution of packets of various sizes" (col. 7, lines 12-16). Applicants submit, however, that this is not equivalent to segmenting packet data into variable size burst units as the mere mention of packets of various sizes does not equate to segmenting packet data. In this regard, *Sah* fails to disclose this feature.

As an independent basis for patentability, *Sah* also fails to disclose ***sequencing a plurality of burst unit memory write operations ensuring that each burst unit memory write operation writes packet data to a memory bank different from the previous burst unit memory write operation***. The Office Action refers to "contiguous address requests" disclosed in the *Sah* reference. (*See, e.g.*, col. 12, lines 14-15: "A stream may comprise a sequence of contiguous address requests to an I/O hub 120A or 120B.") The Office Action also refers to "previously activated page" disclosed by *Sah*. In particular, *Sah* discloses "the second request may be delayed for the duration to close the previously activated page before activating the page for the next request." (Col. 13, lines 51-53). Applicants submit that neither "contiguous address requests" nor the "previously activated page" relate to sequencing a plurality of burst unit memory write operations ensuring that each burst unit memory write operation writes packet data to a memory bank different from the previous burst unit memory write operation. Moreover, the secondary *Ross* reference fails to address the deficiencies in the *Sah* reference.

Accordingly, Applicants respectfully submit that independent claim 1 patently defines over *Sah* in view of *Ross* for at least the reason that the combination fails to disclose, teach or suggest the highlighted features in claim 1 above. In addition, Applicants submit that dependent claims 9-20 are allowable for at least the reason that

these claims depend from an allowable independent claim. *See, e.g., In re Fine*, 837 F. 2d 1071 (Fed. Cir. 1988).

II. Rejection of Claims 15 and 18-20

While Applicants submit that dependent claims 15 and18-20 are allowable for at least the reason that these claims depend from an allowable independent claim, Applicants respectfully object to the rejection of these claims. Regarding these claims, the Office Action asserts the following:

> *8. Claim 15 Sah-Ross disclose preferentially scheduling read burst units corresponding to packets from one of: a packet to be transmitted via a high bandwidth output port, a high quality-of-service packet, a packet of a particular type of service, an alarm packet, and a signaling packet as inherent feature of scheduling.*
>
> *11. Claim 18 Sah-Ross disclose segmenting packet data into at least four as inherent feature of segmenting.*
>
> *12. Claim 19 Sah-Ross disclose segmenting packet data into burst units transferring at least 49 bytes of packet data as inherent feature of segmenting.*
>
> *13. Claim 20 Sah-Ross disclose employing windows at least 128 memory access cycles long as inherent feature of window protocol.*

(Office Action, page 5). Applicants respectfully traverse the finding of inherency and respectfully submit that inherency has not been established. It is well established that "[t]o establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing

may result from a given set of circumstances is not sufficient." *In Re Anthony J. Robertson*, 169 F.3d 743, 745, 49 U.S.P.Q.2D (BNA) 1949, 1950-51 (Fed. Cir. 1999).

III. New Claims 21-27

Applicants submits that new claims 21-27 are allowable over the cited references. Specifically, independent claim 21 is allowable for at least the reason that the cited references do not disclose, teach, or suggest ***segmenting packet data into variable size burst units based on a predefined rule***. The cited references also fail to disclose, teach, or suggest arranging the plurality of sequenced bust unit memory read operations in a plurality of read windows, ***wherein the windows are at least a predetermined minimum size***.

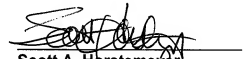
Independent claim 25 is allowable for at least the reason that the cited references do not disclose, teach, or suggest ***means for partitioning packet data, wherein the partitioned packet data size falls between a predetermined minimum and a predetermined maximum burst unit size***. Dependent claims 22-24 and 26-27 are allowable over the cited references for at least the reason that these claims depend from allowable claims. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q. 2d 1596, 1598 (Fed. Cir. 1988).

CONCLUSION

Applicants respectfully submit that all pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephone conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 50-0835.

Respectfully submitted,



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